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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/601,274	06/19/2003	Alberto Baroncelli	B-322	6437

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EXAMINER	
BRIER, JEFFERY A	

ART UNIT	PAPER NUMBER
2672	

DATE MAILED: 10/18/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/601,274	BARONCELLI ET AL.	
	Examiner	Art Unit	
	Jeffery A. Brier	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *09 August 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-14* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-14* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *19 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Detailed Action

Response to Amendment

1. The amendment filed on 8/9/2005 has been entered. The examiner notes claims 12-15 have been renumbered as claims 11-14.

Response to Arguments

2. Applicants arguments filed on 8/9/2005 have been fully considered, however, they are deemed not to be persuasive. The claims are mostly a list of parts having function with no interconnections, thus, a reference that teaches the broad function of the parts and includes the parts teaches the claim. Since claims 4 and 6-14 have significant claim form issues then the arguments concerning these claims are further not persuasive because these claims are poorly connected to their parent claims.

The argument at page 9 third paragraph does not overcome Koselj because Koselj teaches a hardware vector graphics engine, see paragraph 0017.

The argument at page 9 fourth paragraph does not overcome Koselj because Koselj teaches paragraph 0017 teaches sending vector graphics commands to the graphics engine from the CPU and since the claims do not exclude the vector graphics commands of the type found in paragraph 0097. The claim does not define the type of object data that is received and the vector graphics commands of Koselj are object data that define polygonal objects.

The argument in the paragraph spanning pages 9 to 10 does not overcome Koselj because applicants claims are open ended comprising claims, thus, additional teachings of Koselj does not prevent Koselj from teaching the claimed invention.

The argument at page 10 first full paragraph does not overcome Koselj because this paragraph does not address any claim limitations.

The argument at page 10 second full paragraph does not overcome Koselj because Koselj teaches a hardware vector graphics engine that is associated with a display driver unit. Since applicants claims are open ended comprising claims, then the additional teachings of a display unit do not prevent Koselj from teaching the claimed invention.

The argument at page 10 third full paragraph to page 12 second full paragraph and the paragraph spanning pages 12 to 13 does not overcome Koselj because claim 6 does not claim X edger sorting.

The argument at page 12 third full paragraph does not overcome Koselj because claims 2-5 do not claim the argued display list illustrated in the illustration on page 12.

The argument at page 13 first full paragraph to page 14 last full paragraph does not overcome Koselj because Koselj teaches using a hardware circuit and because claim 7 does not claim clock cycles.

The argument in the paragraph spanning pages 14 and 15 regarding claim 8 does not overcome Koselj because the argued limitations are not present in the claim 8 or any claim.

The argument in the first to third full paragraphs on page 15 regarding claim 9 does not overcome Koselj because the argued limitations are not present in the claim 9 or any claim.

The argument in the paragraph spanning pages 15 and 16 to the second full paragraph regarding claim 10 does not overcome Koselj because the argued limitations are not present in the open ended comprising claim 10 or any claim. Claim 10 does not exclude rewriting graphic commands to the vector graphics unit.

The remaining argument on page 16 regarding claims 11-14 do not overcome Koselj because the argued edge curve subdivision is not claimed.

The following is an analysis of claims 4 and 6-10 detail the formal errors in these claims which further enhances the position that these claims are broadly a collection of non-interconnected parts.

Claim 4:

At line 3 the "color ramp data list" does not have corresponding description in the specification. Is the color ramp lookup table the newly claimed color ramp data list.

Claim 6:

At line 8 "the address" refers to an address that was not previously claimed in claim 6 or 1, thus, this is a non-related part to claim 1.

Claim 7:

At line 8 "the address locations" refers to an address that was not previously claimed in claim 7 or 1, thus, this is a non-related part to claim 1.

Claim 8:

At line 8 "the weight factor" refers to a factor that was not previously claimed in claim 8 or 1, thus, this is a non-related part to claim 1.

Claim 9:

At line 5 "the active edge" refers to an active edge that was not previously claimed in claim 9 or 1, thus, this is a non-related part to claim 1. At line 7 "the weight factor" was not previously claimed in claim 9 or 1, thus, this is a non-related part to claim 1. At line 9 "a dump buffer" is recited and in claim 1 a dump buffer hardware circuit is recited. Are these the same or different? If they are different then once again the claims claim a collection of non-related parts.

Claim 10:

At line 6 "an antialiasing and transparence factors" is claimed but grammatically this should be "an antialiasing factor and a transparence factor" or "antialiasing and transparence factors". At line 8 "the color pixel value", at line 12 "the dump buffer", and at line 13 "the red, green, blue value" were not previously claimed in claims 9 or 1, thus, these claimed terms are non-related parts to claim 1. At line 13 the word "again" refers to a previous read while such a read was not previously claimed. At line 15 the word "again" refers to a previous write while such a write was not previously claimed.

Claims 11, 12, and 13:

At line 2 "a Bezier hardware circuit" is claimed and in parent claim 1 "a Bezier hardware circuit" is claimed, thus, this is a non-related part to claim 1.

Claim 14:

At line 31 "the address" refers to an address that was not previously claimed in claim 14, thus, this is a non-related part to the remaining parts of claim 14. At line 33 "an dual port memory" should be rewritten as "a dual port memory". At line 43 "the weight factor" refers to a factor that was not previously claimed in claim 14, thus, this is a non-related part to claim 1. At line 48 "a dump buffer" is recited and in claim 14 a dump buffer hardware circuit is recited. Are these the same or different? If they are different then once again the claims claim a collection of non-related parts. At lines 53-54 "an antialiasing and transparence factors" is claimed but grammatically this should be "an antialiasing factor and a transparence factor" or "antialiasing and transparence factors". At line 55 "the color pixel value", at line 59 "the dump buffer", and at line 60 "the red, green, blue value" were not previously claimed in claim 14, thus, these claimed terms are non-related parts to claim 14. At line 61 the word "again" refers to a previous read while such a read was not previously claimed. At line 62 the word "again" refers to a previous write while such a write was not previously claimed.

From the above it is clear the claims are a collection of non-connected parts which parts are taught by the Koselj et al. reference.

Drawings

3. The drawings are objected to because figures 4, 5, 6, 7, and 8 should have their separate views labeled as separate figures such as figure 4(a) since the specification describes them as separate figures. Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

4. The rejection set forth in the last office is action is reproduced below for convenience. The only changes reflects the renumbering of the claims and amendments.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

6. Claims 1-14 are rejected under 35 U.S.C. 102(e) as being anticipated by Koselj et al (US 2003/0214506).

Regarding claim 1, Koselj et al discloses that the claimed feature of a vector graphics circuit for rendering vector and bitmap graphics objects to a final image, the vector graphics circuit comprising: a. an input display list memory [10] for receiving an input stream of object (*This broad claim limitation does not express or manifest any specific type of object data that may be different than that which Koselj teaches to one of ordinary skill in the art.*) data (See Fig 1, Fig 2, Fig 21); b. a sorting hardware circuit for optimizing the scan conversion algorithm (See Fig 17, [11]); c. a Bezier hardware circuit [11] for vector curve subdivision (See Fig 1-2, Fig 7-8, Fig 17, Fig 21,

[48],[91],[138-141], claim 24); d. an antialiasing hardware circuit for calculating sub-pixel values (See [26],[32-40],[96]); e. a color hardware circuit [7] for reordering and for optimizing the access to a plurality of bitmaps and mathematical tables inside the display list memory (See Fig 1, Fig 17, Fig 21); f. a dump buffer [13,15,17] hardware circuit, using a memory, which composes the vector graphics objects in a final pixel bitmap. (See Fig 1, Fig 17, Fig 21, [93],[244],[247])

Regarding claim 2, Koselj et al discloses that the input display list memory is arranged to include a quadratic or cubic Bezier edge data list. (See Fig 7, [138-141])

Regarding claim 3, Koselj et al discloses that the input display list memory is arranged to include a color data list. (See [30-32],[89],[93],[247])

Regarding claim 4, Koselj et al discloses that the input display list memory is arranged to include a color ramp data list. (See [30-32],[89],[93],[247])

Regarding claim 5, Koselj et al discloses that the input display list memory is arranged to include a pattern or bitmap data list. (See [7-8],[213])

Regarding claim 6, Koselj et al discloses that the sorting hardware circuit comprises: a. an active edge processor subunit that stores the edges of a current scan line inside an active edge table with increasing X, the active edge table comprises a

dual port memory, where two alternating ping-pong buffers are stored; b. a free active edge stack acting as a LIFO stack, to generate the address of the active edge table. (See Fig 1, Fig 17, Fig 21)

Regarding claim 7, Koselj et al discloses that a Bezier hardware circuit store a series of segments inside an dual port memory comprising: a. a subdivided Bezier parameter unit, comprising three couples of X and Y adders/divide by two, plus a delay element; b. a De Casteljau subdivision unit; c. a Bezier subdivision tree address unit that generates the address locations of the Bezier segments inside a dual port memory. (See Fig 1-2, Fig 7-8, Fig 17, Fig 21, [48],[91],[138-141], claim 24)

Regarding claim 8, Koselj et al discloses that the antialiasing hardware circuit computes the number of sub-pixels present in a N=i*4 real pixels per clock, to obtain the weight factor used for a scan-converted row. (See [33],[96])

Regarding claim 9, Koselj et al discloses that the color hardware circuit includes: a. a color generator subunit that outputs a solid or a processed color when a linear gradient, a radial gradient a tiled bitmap or a clipped bitmap are associated with the active edge (See Fig 9-10, [151-156]); b. a color composer subunit that uses the weight factor to process the color from the color generator and store the result in to a dump buffer. (See [93],[244],[247])

Regarding claim 10, Koselj et al discloses that the buffer hardware circuit stores a pixel region into a buffer, where all the objects are composed, comprising: a. a fixed single line dump buffer memory that stores the color pixels processed by an antialiasing and transparence factors; b. a store buffer memory that stores the color pixel value using the following algorithm: i. Read the background pixel from the store buffer memory, multiply it by the complementary of the transparence (1-alpha), obtained from the dump buffer, and add it with the red, green, blue values again from the dump buffer. ii. the result is written again inside the store buffer. (See Fig 1, Fig 17, Fig 21, [151])

Regarding claim 11, claim 11 is similar in scope to the claim 7, and thus the rejection to claim 7 hereinabove is also applicable to claim 11.

Regarding claim 12, claim 12 is similar in scope to the claim 7, and thus the rejection to claim 7 hereinabove is also applicable to claim 12.

Regarding claim 13, claim 13 is similar in scope to the claim 7, and thus the rejection to claim 7 hereinabove is also applicable to claim 13.

Regarding claim 14, claim 14 is similar in scope to the combination of claims 1-10, and thus the rejections to claims 1-10 hereinabove are also applicable to claim 14.

7. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffery A Brier whose telephone number is (571) 272-7656. The examiner can normally be reached on M-F from 7:00 to 3:30. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi, can be reached at (571) 272-7664. The fax phone Number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should

you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jeffery A Brier
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Art Unit 2672